AMENDMENTS TO THE CLAIMS

Claim 1 (Withdrawn): A method for building a time-sliced architecture in a spread spectrum system, comprising the steps of:

(a) analyzing a set of applications, said analyzing including the steps of:

(i) extracting real time aspects from each application in said set of applications;

(ii) determining an optimal granularity based on said real time aspects; and

(iii) adjusting said optimal granularity based on a context switching overhead; and

(b) building a specific time-sliced architecture to accommodate said range of applications based on said analyzing.

Claim 2 (Withdrawn): The method of claim 1, wherein said extracting includes the step of:

profiling fundamental processing elements in each application in said set of applications.

Claim 3 (Withdrawn): The method of claim 1, wherein said determining includes the step of:

determining a lowest level of granularity needed for each application in said set of applications.

Claim 4 (Withdrawn): The method of claim 1, wherein said adjusting includes the step of:

performing a sensitivity analysis.

Claim 5 (Withdrawn): The method of claim 4, wherein said performing includes the step of:

determining an optimal trade-off between said context switching overhead and said optimal granularity.

Claim 6 (Withdrawn): The method of claim 1, wherein said building includes the steps of:

determining a size for a data cache based on said extracting;

implementing a hierarchical caching structure in said data cache; and

applying said data cache in said specific time-sliced architecture.

Claim 7 (Withdrawn): A computer program product for building a time-sliced architecture in a spread spectrum system, comprising:

(a) logic code for analyzing a set of applications, said logic code for analyzing including:

(i) logic code for extracting real time aspects from each application in said set of applications;

(ii) logic code for determining an optimal granularity based on said real time aspects; and

(iii) logic code for adjusting said optimal granularity based on a context switching overhead; and

(b) logic code for building a specific time-sliced architecture to accommodate said range of applications based on said analyzing.

Claim 8 (Withdrawn): The computer program product of claim 7, wherein said logic code for extracting includes:

logic code for profiling fundamental processing elements in each application in said set of applications.

Claim 9 (Withdrawn): The computer program product of claim 7, wherein said logic code for determining includes:

logic code for determining a lowest level of granularity needed for each application in said set of applications.

Claim 10 (Withdrawn): The computer program product of claim 7, wherein said logic code for adjusting includes:

logic code for performing a sensitivity analysis.

Claim 11 (Withdrawn): The computer program product of claim 10, wherein said logic code for performing includes:

logic code for determining an optimal trade-off between said context switching overhead and said optimal granularity.

Claim 12 (Withdrawn): The computer program product of claim 7, wherein said logic code for building includes:

logic code for determining a size for a data cache based on said extracting;

logic code for implementing a hierarchical caching structure in said data cache; and

logic code for applying said data cache in said specific time-sliced architecture.

Claim 13 (Previously Presented): A time-sliced processor for use in a communication system comprising:

a master control unit including a time slot table and a partial sum table for any time slot granularity;

a data cache for receiving input data and for caching intermediate data; and

a plurality of signal processing elements, each element comprising:

a cache for receiving data from the data cache and for caching intermediate data,

a data selector connected to an output of the cache,

a symbol computing engine connected to an output of the data selector, and

a symbol integrator connected to an output of the symbol computing engine.

Claim 14 (Withdrawn): The method of claim 1, wherein the method is independent of a communication protocol.

Claim 15 (Withdrawn): The computer program product of claim 7, wherein the computer program product is independent of a communication protocol.

Claim 16 (Previously Presented): The time-sliced processor of claim 13, wherein the time-sliced processor is independent of a communication protocol.

Claim 17 (Previously Presented): The time-sliced processor of claim 13, wherein the communication system is a spread-spectrum communication system.

Claim 18 (Previously Presented): The time-sliced processor of claim 17, wherein the time-sliced processor supports multiple spread spectrum applications that run at different granularities when optimized.

Claim 19 (Previously Presented): The time-sliced processor of claim 13, wherein the signal processing elements are finger processing elements.

Claim 20 (Previously Presented): The time-sliced processor of claim 13, wherein the symbol computing engine is a despreader.

Claim 21 (Previously Presented): The time-sliced processor of claim 13, wherein the master control unit configures and controls the data cache and the signal processing elements.

Claim 22 (Previously Presented): The time-sliced processor of claim 13, wherein the master control unit schedules time-sliced signal processing in the data cache and the signal processing elements.

Claim 23 (Previously Presented): The time-sliced processor of claim 13, wherein the master control unit allocates time slots, maintains synchronization of the signal processing elements, and maximizes throughput.

Claim 24 (Previously Presented): The time-sliced processor of claim 13, wherein the master control unit allocates the partial sum table on a per signal processing element basis to extend signal processing control flexibility across time slots.

Claim 25 (Previously Presented): The time-sliced processor of claim 13, wherein the master control unit is linked to an external processing element to manage time slot allocation among the signal processing elements.

Claim 26 (Previously Presented): The time-sliced processor of claim 13, wherein the time-sliced processor calls programming across different protocols in a given application space.

Claim 27 (Previously Presented): The time-sliced processor of claim 13, wherein the time-sliced processor performs speed grading of components.

Claim 28 (Previously Presented): A master control unit in a time-sliced processor of a communication system having a data cache, which receives input data and caches intermediate data, and a plurality of signal processing elements, the master control unit comprising:

a time slot table; and

a partial sum table,

wherein the master control unit configures and controls the data cache and the signal processing elements for any time slot granularity.

Claim 29 (Previously Presented): The master control unit of claim 28, wherein the master control unit schedules time-sliced signal processing in the data cache and the signal processing elements.

Claim 30 (Previously Presented): The master control unit of claim 28, wherein the master control unit allocates time slots, maintains synchronization of the signal processing elements, and maximizes throughput.

Claim 31 (Previously Presented): The master control unit of claim 28, wherein the master control unit allocates the partial sum table on a per searcher basis to extend search control flexibility across time slots.

Claim 32 (Previously Presented): The master control unit of claim 28, wherein the master control unit is linked to an external processing element to manage time slot allocation among the signal processing elements.

Claim 33 (Previously Presented): The master control unit of claim 28, wherein the communication system is a spread-spectrum communication system.

Claim 34 (Previously Presented): The master control unit of claim 22, wherein master control unit enables the time-sliced processor to support multiple spread spectrum applications that run at different granularities when optimized.

Claim 35 (Previously Presented): The master control unit of claim 28, wherein the master control unit enables the time-sliced processor to call programming across different protocols in a given application space.

Claim 36 (Previously Presented): The master control unit of claim 28, wherein the master control unit enables the time-sliced processor to perform speed grading of components.

Claim 37 (Previously Presented): A time-sliced processor for use in a communication system comprising:

a data cache for receiving input data and for caching intermediate data;

a plurality of signal processing means, each signal processing means comprising:

a cache for receiving data from the data cache and for caching intermediate data,

a data selecting means connected to an output of the cache,

a symbol computing means connected to an output of the data selecting means, and

a symbol integration means connected to an output of the symbol computing means;

and

a master control means, including a time slot table and a partial sum table, for configuring and controlling the data cache and the signal processing means for any time slot granularity.

Claim 38 (Previously Presented): The time-sliced processor of claim 13, wherein the partial sum table completes a signal processing function across multiple time slots.

Claim 39 (Previously Presented): The time-sliced processor of claim 13, wherein the data cache caches intermediate data for completing a signal processing function across multiple time slots.

Claim 40 (Previously Presented): The master control unit of claim 28, wherein the partial sum table completes a signal processing function across multiple time slots.

Claim 41 (Previously Presented): The master control unit of claim 28, wherein the master control unit allocates the partial sum table on a per signal processing element basis to extend signal processing control flexibility across time slots.

Claim 42 (Previously Presented): The time-sliced processor of claim 13, wherein the time slot granularity is at chip boundary.

Claim 43 (Previously Presented): The time-sliced processor of claim 13, wherein the time slot granularity is at sub-chip boundary.

Claim 44 (Previously Presented): The master control unit of claim 28, wherein the time slot granularity is at chip boundary.

Claim 45 (Previously Presented): The master control unit of claim 28, wherein the time slot granularity is at sub-chip boundary.

Claim 46 (Previously Presented): The time-sliced processor of claim 37, wherein the time slot granularity is at chip boundary.

Claim 47 (Previously Presented): The time-sliced processor of claim 37, wherein the time slot granularity is at sub-chip boundary.